JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **5** No 1, 01017(5pp) (2013)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **5** № 1, 01017(5cc) (2013)

Performance of a Double Gate Nanoscale MOSFET (DG-MOSFET) Based on Novel Channel Materials

Rakesh Prasher, Devi Dass, Rakesh Vaid*

Department of Physics & Electronics, University of Jammu, Jammu-180006

(Received 08 December 2012; revised manuscript received 26 January 2013; published online 28 March 2013)

In this paper, we have studied a double gate nanoscale MOSFET for various channel materials using simulation approach. The device metrics considered at the nanometer scale are subthreshold swing (SS), drain induced barrier lowering (DIBL), on and off current, carrier injection velocity (v_{inj}), etc. The channel materials studied are Silicon (Si), Germanium (Ge), Gallium Arsenide (GaAs), Zinc Oxide (ZnO), Zinc Sulfide (ZnS), Indium Arsenide (InAs), Indium Phosphide (InP) and Indium Antimonide (InSb). The results suggest that InSb and InAs materials have highest I_{on} and lowest I_{off} values when used in the channel of the proposed MOSFET. Besides, InSb has the highest values for I_{on} / I_{off} ratio, v_{inj}, transconductance (g_m) and improved short channel effects (SS = 59.71 and DIBL = 1.14, both are very close to ideal values). More results such as effect of quantum capacitance verses gate voltage (V_{gs}), drain current (I_{ds}) vs. gate voltage and drain voltage (V_{ds}), ratio of transconductance (g_m) and drain current (I_d) vs. gate voltage, average velocity vs. gate voltage and injection velocity (V_{inj}) for the mentioned channel materials have been investigated. Various results obtained indicate that InSb and InAs as channel material appear to be suitable for high performance logic and even low operating power requirements for future nanoscale devices as suggested by latest ITRS reports.

Keywords: Channel materials, Ballistic nanoscale MOSFET, Gate insulator thickness, Insulator dielectric constant, Gate control parameter, Drain control parameter, Indium antimonide.

PACS numbers: 85.30.De, 85.30.Tv

1. INTRODUCTION

There is considerable interest these days in exploring the use of alternative channel materials in ballistic nanoscale MOSFETs. New materials in the channel in place of silicon reduce series resistance, enhance on-current and improve transport properties. ITRS 2003 predicts that novel MOSFETs with gate lengths up to 9 nm will be produced by 2016. It is expected that novel MOSFETs will be operated near ballistic scale because the channel length of MOSFETs will be comparable to or shorter than the mean free path of a carrier [1-3]. Beyond that we need to have high k dielectric materials as replacement for silicon dioxide. Si-SiO_2 has excellent interface properties, but silicon has poorest transport properties like mobility and diffusion constant. Results show much higher electron mobility than Si if InSb (Indium Antimonide) is used as channel material and it provides 50 % performance improvement and up to 10x power reduction. InSb is an interesting material because of its high electron mobility appropriate for high speed transistors [4] and Hall-effect devices. Its narrow band gap is also suitable for the infrared applications. InSb can directly be grown on Si substrate without insertion of buffer layer and leakage current between InSb and Si Substrate is very small [5].

A Double-Gate (DG) MOSFET as shown in Fig. 1, offers distinct advantage for scaling to have improved gate-channel control for reducing of short-channel effects (SCEs). Since all the drain field lines are not able to reach the source [6], the gate oxide has a lower dielectric constant than Si (assuming the oxide is SiO_2) due to ultra thin body. Because of its greater resilience to SCEs and greater gate channel control, the physical gate thickness can be increased (compared to planar MOSFET). Thus, it also brings along reduced leakage currents (gate leakage as well as S/D leakage). DG-MOSFET is one of the promising technologies for transistor design. To accommodate future technology nodes, transistor dimensions have to be reduced which leads to several disadvantages in transistor function. By using double-gate transistors many of these problems can be resolved to give efficient circuit performance [7].

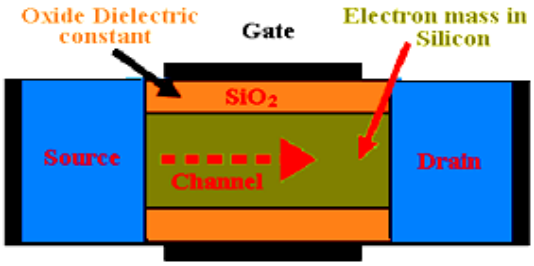

Fig. 1 – Cross section of a generic planar DG n-MOSFET

In a truly ballistic transistor, the on-current per unit device width (I_{on}) is given by the inversion density N_{inv} times the average injection velocity v_{inj} at the virtual source. Hence, the ballistic current depends on the transport masses, on the number of valleys in the two-dimensional (2-D) Brillouin zone, and on the transport direction with respect to the principal axes of the valleys. In other words, the ballistic current is affected by the channel material, the wafer orientation (that sets the quantization direction normal to the semiconductor-dielectric interface), and by the channel direction in

* rakeshvaid@ieee.org

the transport plane. I_{on} is given in terms of technological and channel material parameters by the following expression:

$$I_{on} = \frac{8qh}{3\sqrt{\pi}} \frac{(N_{inv})^{\frac{3}{2}}}{(n_v)^{\frac{1}{2}}(m_w)^{\frac{1}{4}}(m_L)^{\frac{3}{4}}} \quad (1),$$

where n_v is the valley degeneracy, while m_L and m_w are the effective masses in the direction of the channel length and width, respectively. The expression given in (1) suggests that the maximum I_{on} is obtained for the smallest transport masses and valley degeneracy, hence, for III–V materials such as GaAs, InP, InAs, InSb etc.

A high mobility channel material has high injection velocity to increase the on-state current and it also reduces delay. Currently, strained-Si is the dominant technology for high performance MOSFETs and increasing the strain provides a viable solution to scaling. Due to their extremely small transport mass leading to high injection velocity (v_{inj}), III-V compounds appear to be very attractive candidates as channel materials for highly scaled n-MOSFETs [8]. However, III-V materials have many significant and fundamental issues, which may prove to be severe bottlenecks to their implementation. Although their small transport mass leads to high v_{inj}, III-V materials have a low density of states (DOS) in the Γ-valley, tending to reduce the inversion charge (Q_{inv}) and hence reduce drive current [9, 10]. Furthermore, the small direct band gaps of Ge and III-V materials inherently give rise to very large band to band tunneling (BTBT) leakage current compared to Si. Despite of low inversion charge (Q_{inv}), due to their large injection velocity (v_{inj}), III-V materials like InAs, InSb and InP can have larger drive current than Si up to 80 %. The I_{off}, BTBT in Ge, InAs, GaAs and InSb can be reduced by over ~ 1000X by scaling. III-V materials have significantly smaller effective mass and higher electron mobility compared to Si and Ge. Due to the increasing electric-fields in the channel and the smaller bandgap as shown in Fig. 2, the BTBT leakage current can become excessive and can ultimately limit the scalability of high mobility channel materials [8, 11, 12].

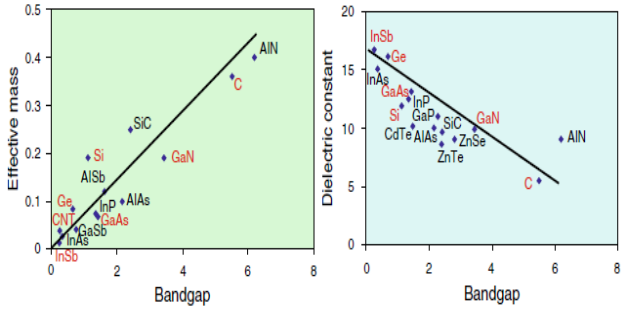

Fig. 2 – Tradeoffs between effective mass, bandgap, and dielectric constant in semiconducting materials

In this paper, we have made a comparative study by using different channel materials like Ge, ZnO, ZnS, GaAs, InP, InAs and InSb in place of silicon. Various simulation results obtained suggest that InAs and InSb have many advantages that make them suitable to use as channel material in future nanoscale MOSFETs.

Table 1 – Properties of various important channel materials used

	Compound Semiconductors					
	Si	Ge	InP	GaAs	InAs	InSb
Effective Mass	0.19	0.82	0.077	0.063	0.028	0.014
Electron mobility(μ_s) Cm^2 / v-s	1450	3900	5900	9200	33000	77000
Band Gap (eV)	1.12	0.66	1.34	1.42	0.35	0.17
Lattice Constant(Å)	5.43	5.65	5.86	5.65	6.05	6.47
Valley degeneracy	2	1	1	1	1	1

2. SIMULATION DETAILS

In order to examine the ballistic transport properties of a nanoscale MOSFET, the simulation and modeling in this paper was achieved through FETToy. 2.0 is a numerical simulator which uses a set of Matlab scripts to calculate ballistic I-V characteristics for conventional single- and double-gate geometry MOSFETs, nanowire MOSFETs, and carbon nanotube MOSFETs based on the Natori (or "top-of-the-barrier") approach [13].

Table 2 – Input parameter used for different channel materials

S. No.	Input Parameters	Value
1	t_{ins}	5 nm
2	k_{ins}	3.9
3	T	300 K
4	V_{th}	0.32 eV
5	α_G	1.00
6	α_D	0

3. RESULTS AND DISCUSSION

3.1 $I_{ds} - V_{ds}$ Characteristics

Fig. 3 show I_{ds}-V_{ds} plots at constant V_{gs} = 1 volt and t_{ins} = 5 nm for different channel materials. Exact saturation occurs around 0.083 volts to 0.58 volts for all the channel materials. Ge and ZnS get saturated almost at the same voltage of 0.083 volts, ZnO and Si gets saturated at 0.16 volts, InP and GaAs are saturated

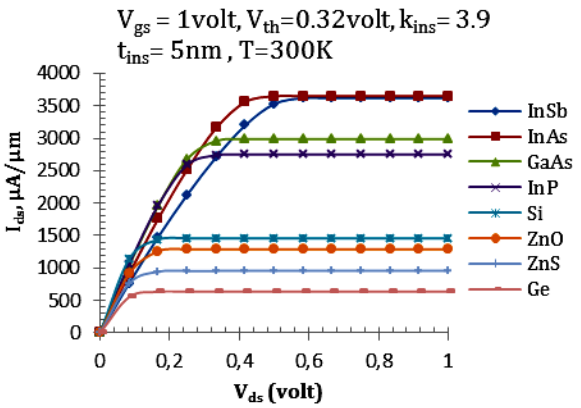

Fig. 3 – Variations of Drain current and Drain voltage for different channel materials

between 0.25 to 0.333 volts. InAs gets saturated at 0.41 volts and finally InSb get saturated at 0.58 volts. InAs and InSb have higher saturation current around 3.56 mA/μm. Ge, ZnO, ZnS and Si curves saturate at low drain current and drain voltage. On the whole this figure indicates that III-V materials have more current density as compared to Si and Ge, which is highly desired for channel material.

3.2 I_{ds} – V_{gs} Characteristics

Fig. 4 shows the I_{ds} versus V_{gs} curves at constant V_{ds} of 1 volt and t_{ins} of 5 nm for different channel materials. InAs and InSb shows higher drain current but it requires lower threshold voltage, thus it is not possible

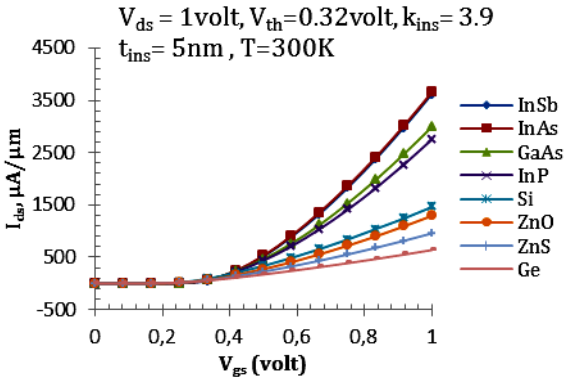

Fig. 4 – Variations of Drain current and gate voltage for different channel materials

to suppress subthreshold effects and quantum confinement cannot be achievable. Therefore, germanium and silicon with strained and unstrained materials are preferable for given threshold voltage and optimum drain current. Higher channel leakage current is possible in InAs and InSb so that we can use stained InSb and strained InAs in place of unstrained materials.

3.3 Quantum capacitance w. r. t. gate voltage

Fig. 5 shows that all channel materials have similar quantum capacitance verses gate voltage behavior. The device can be operated at quantum capacitance limit

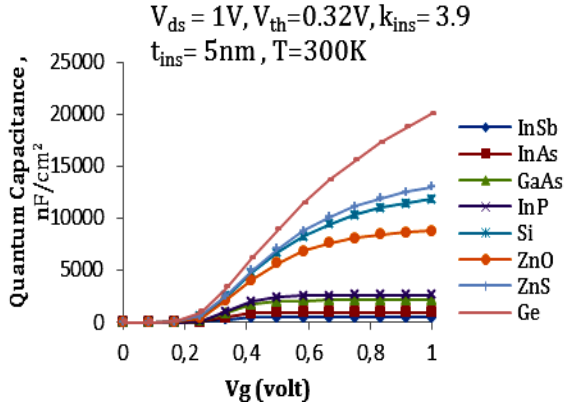

Fig. 5 – Variations of Quantum Capacitance and gate voltage for different channel materials

when its gate capacitance is considerably higher than quantum capacitance. To know device operation at QCL limit, value of quantum capacitance at inversion, depletion and accumulation regions, and the study of $Q_c - V_g$ curves are drawn. For InAs at low voltage (up to V_g = 0.166 volts) quantum capacitance remains constant i.e. 2.50 nf / cm^2. There is linear relationship between quantum capacitance and drain voltage up to V_g = 0.5 volt and finally its get saturated. $Q_c - V_g$ curve of Silicon has low quantum capacitance of 0.32 nf / cm^2 with threshold voltage around 0.166 volts. But InAs and InSb have well defined accumulation and inversion regions with higher threshold voltage due its higher gate capacitance and quantum capacitance of 2.5 nf/cm^2.

3.4 g_m / I_d w. r. t. gate voltage

Fig. 6 shows (g_m / I_d) variations w. r. t. gate voltage at constant drain voltage (V_{ds} = 1 volt) and gate oxide thickness (t_{ins} = 5 nm) for different channel materials. In this graph, we can see that as the V_{gs} increases the g_m / I_d decreases, in other words, the transconductance of the device (g_m) decreases for the current polarization by governing the equation, $g_m = I_d / V_{gs}$. In this figure, for InSb g_m / I_d ratio remains constant up to V_{gs} = 0.166 volts and after that it decreases and follows almost polynomial equation of the order 6. As we know the maximum performance can be obtained when the value of g_m / I_d ratio is the largest. InSb and InAs shows higher transconductance efficiency than the other channel materials in DG n-MOSFET.

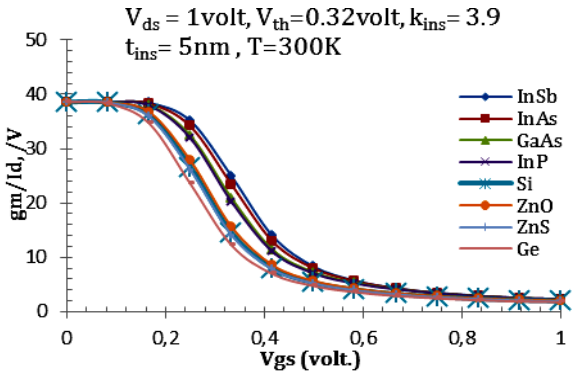

Fig. 6 – Variations of g_m / I_d and gate voltage for different channel materials

3.5 Average velocity w. r. t. gate voltage

Fig. 7 shows average velocity variations w. r. t. gate voltage at constant drain voltage (V_{ds} = 1 volt) and gate oxide thickness (t_{ins} = 5 nm) for different channel materials. In this figure, when no gate voltage (V_{gs} = 0 volt) is applied the average velocity of InSb is maximum because it has less effective mass as compare to other channel materials. For a certain change in gate voltage the average velocity approaches to zero. It means gate voltage does not affect average velocity.

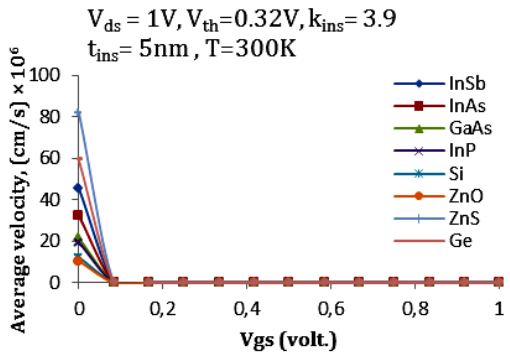

Fig. 7 – Variations of Average velocity and gate voltage for different channel materials

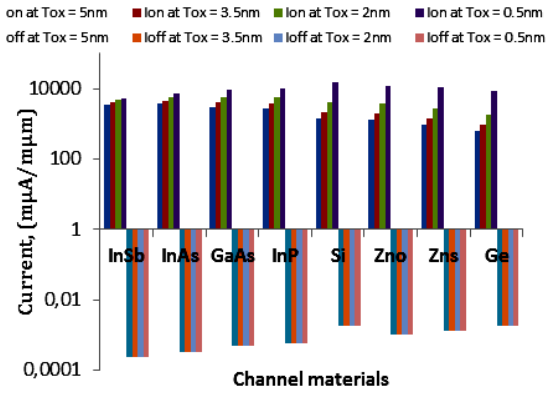

Fig. 8 – Variations of Current (I_{on} & I_{off}) with different channel materials at various oxide thicknesses

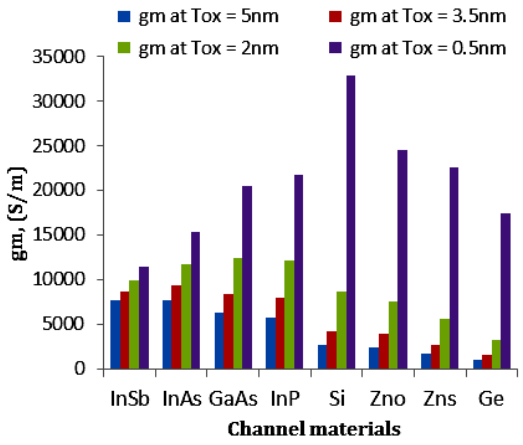

Fig. 9 – Variations of Transconductance (g_m) with different channel materials at various oxide thicknesses

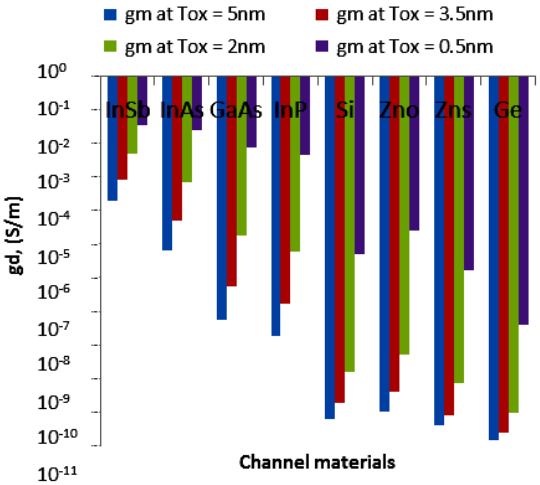

Fig. 10 – Variations of Output conductance (g_d) with different channel materials at various oxide thicknesses

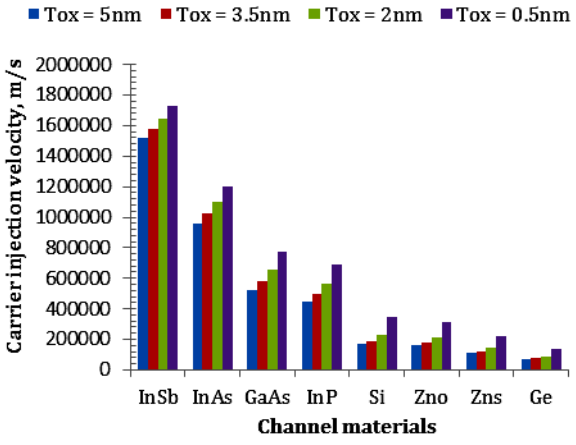

Fig. 11 – Variations of Carrier injection velocity with different channel materials at various oxide thicknesses

4. CONCLUSIONS

On the basis of various results obtained using simulation approach, we conclude the following:

– Indium Arsenide has highest I_{on} (3.65×10^3 nA / nm and 4.33×10^3 nA / nm) and lowest I_{off} as compared to other channel materials at gate insulator thickness (t_{ins}) = 5 nm and 3.5 nm resp. whereas at other gate oxide thickness GaAs has highest I_{on}.

– InAs has highest transconductance (g_m) as compared to other channel materials for gate insulator thickness (t_{ins}) = 5 nm and 3.5 nm whereas at other gate oxide thickness GaAs has highest transconductance.

– InSb has highest output conductance (g_d) at different values of oxide thickness. Higher transconductance means gate has more control over the charge in the channel.

– Carrier injection velocity of InSb and InAs is bigger as compared to other channel materials. It means the mobility of charge carrier in these materials is higher due to which they give higher I_{on}.

– Finally, InAs has threshold swing of 59.70, highest I_{on}, highest transconductance, as well as maximum carrier mobility. III-V compound materials show better performance than other channel materials (II-VI, Ge, Si etc.) when used in DGMOSFET.

REFERENCES

1. Anisur Rahman, Jing Guo, Supriyo Datta, Mark S. Lundstrom, *IEEE T. Electron Dev.* **50**, 1853 (2003).
2. E.N. Ganesh, K. Ragavan, K. Kumar, *GESJ: Physics* No1 (3), 62 (2010).
3. G. Timp, J. Bude, et al., *IEDM Tech. Digest* 55 (1999).
4. S. Datta, et al, *IEEE IEDM,* 783 (1999).
5. Y. Kunimi et al, *IEEE IEDM,* 853 (2009).
6. D. Flandre et al., *Analog Integr. Circ. S.* **21**, 213 (1999).
7. S. Gupta et al., *International Conference on Electronics Computer Technology (ICECT),* **2**, 33 (2011).
8. R. Chau et al, *IEEE T. Nanotechnol.* **4**, 153 (2005).
9. M. Fischetti, S.E. Laux, *IEEE T. Electron Dev.* **38**, 650 (1991).
10. S. Laux, *IEEE T. Electron Dev.* **54**, 2304 (2007).
11. S. Datta, G. Dewey, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, R. Chau, *Proc. IEEE IEDM*, 653 (2003).
12. T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nishi, K.C. Saraswat, *IEEE T. Electron Dev.* **53**, 990 (2006).
13. K. Natori, *J. Appl. Phys.* **76** (8), 4881 (1994).